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<tr><td>Course Title</td><td>Computer Architecture</td><td>Course No</td><td colspan="5">old COM522</td></tr>
<tr><td rowspan="2">Department/ Specialization</td><td rowspan="2">Computer Science and Engineering</td><td rowspan="2">Credits</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>3</td><td>0</td><td>2</td><td>4</td></tr>
<tr><td>Faculty proposing the course</td><td>Noor Mahammad Sk</td><td>Status</td><td colspan="2">Core □</td><td>Elective</td><td>■</td></tr>
<tr><td>Offered for</td><td>M.Tech, PhD - CSE, ECE</td><td>Type</td><td colspan="2">New □</td><td>Revision</td><td>■</td></tr>
<tr><td>To take effect from</td><td></td><td rowspan="2">Submitted for approval</td><td colspan="4" rowspan="2">_____Senate</td></tr>
<tr><td>Prerequisite</td><td>Computer Organization, Digital System Design</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">The course aims to expose students to the concepts involved in the design of computer systems covering aspects such as instruction sets, pipelining, caches, physical memory, virtual memory, superscalar and out-of-order instruction execution, vector processor and multithreading</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">Students will have the ability to design a computer system addressing issues related to Instruction level, data level and thread level parallelisms.</td></tr>
<tr><td>Course Contents (with approximate breakup of hours for lecture/ tutorial/practice)</td><td colspan="6">Fundamentals of Quantitative, Design and Analysis Computers. (3)
Memory Hierarchy Design: Optimizations of Cache Performance, Memory Technology and Optimizations, Virtual Memory and Virtual Machines. (7)
Instruction-Level Parallelism and Its Exploitation: ILP Concepts and Challenges, Overcoming Data Hazards with Static and Dynamic Scheduling, Reducing Branch Costs with Advanced Branch Prediction, Static and Dynamic Scheduling, Hardware-Based Speculation, Studies of the Limitations of ILP. (10)
Multi-Threading: Exploiting Thread-Level Parallelism to Improve Uniprocessor Throughput (7)
Data-Level Parallelism in Vector, SIMD, and GPU Architectures: Vector Architecture, Detecting and Enhancing Loop-Level Parallelism. (5)
Thread-Level Parallelism: Centralized Shared-Memory Architectures, Performance of Symmetric Shared-Memory Multiprocessors, Distributed Shared-Memory and Directory- Based Coherence, Synchronization, Models of Memory Consistency, Multicore Processors and Their Performance. (5)
Warehouse-Scale Computers to Exploit Request-Level and Data-Level Parallelism: Programming Models and Workloads for Warehouse-Scale Computers, Computer Architecture of Warehouse-Scale Computers, Physical Infrastructure and Costs of Warehouse-Scale Computers, Cloud Computing: The Return of Utility Computing. (5)
Practice Component: Pipelined arithmetic circuits, Five Stage Pipelined Processor, ILP Concepts. (6 Sessions)
Simulation of Branch Prediction, Static Scheduling and Dynamic Scheduling, Cache Mapping Schemes, Cache Coherence Algorithms. (8 Sessions)</td></tr>
<tr><td>Essential Reading</td><td colspan="6">1. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 6th Edition, The Morgan Kaufmann, 2017, ISBN-13: 978-0128119051.</td></tr>
<tr><td>Supplementary Reading</td><td colspan="6">1. John P. Shen and Mikko H. Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors, 1st Edition, Waveland Press, 2013, ISBN-13: 978-1478607830.
2. D.M. Harris and S.L. Harris. Digital Design and Computer Architecture, 2nd Edition. Morgan Kaufmann, 2012, ISBN-13: 978-0123944245.</td></tr>
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